IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Possley

Application No.: not yet assigned

Filed: not yet assigned

For: GATE ARRAY ARCHITECTURE

Examiner: not yet assigned

Art Unit: not yet assigned

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Dear Sir:

The above-referenced patent application is a continuation patent application under 37 CFR 1.53(b). Applicant respectfully requests that the Examiner enter the following amendments and consider the following remarks. A "Marked Version to Show Changes" is attached hereto.

IN THE SPECIFICATION:

Please insert the following new paragraph in the front of the patent application:

This is a Continuation Patent Application of U.S. Patent Application Serial No. 09/262,458, filed March 4, 1999, titled "Gate Array Architecture," by Brian D. Possley, assigned to the assignee of the present application and herein incorporated by reference.

IN THE CLAIMS:

Please cancel claims 1-26.

Please add the following new claims:

27. An integrated circuit comprising: a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least one forming both N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P- type transistors;

the relatively sized P-type diffusions regions being substantially adjacent;

successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions; and

immediately successive rows within similarly-sized diffusion regions have opposite polarity.

28. The integrated circuit of claim 27, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

29. The integrated circuit of claim 28, wherein the ratio between the capacitance of the larger and smaller relatively-sized transistors is on the order of one-third.

30. The integrated circuit of claim 27, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

31. The integrated circuit of claim 30, and further comprising an interconnect overlying said gate array architecture;

the interconnect being adapted to connect the transistors of the gate array architecture to form a flip-flop.

32. The integrated circuit of claim 31, wherein the interconnect is further adapted to connect the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

33. The integrated circuit of claim 32, wherein said gate array architecture is repeated in said integrated circuit.

34. The integrated circuit of claim 32, wherein said integrated circuit is incorporated in a communications device.

35. The integrated circuit of claim 32, wherein said integrated circuit is attached to a motherboard.

36. The integrated circuit of claim 35, wherein said integrated circuit is incorporated in a personal computer.

37. The integrated circuit of claim 36, wherein said personal computer comprises one of a laptop and a desktop computer.

38. An article comprising: a storage medium, said storage medium having instructions stored thereon, said instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least forming both N-type and P-type transistors;

wherein the transistors are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors;

the relatively-sized P-type diffusion regions being substantially adjacent;

successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions; and

immediately successive rows within similarly-sized diffusion regions have opposite polarity.

39. The article of claim 38, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

40. The article of claim 39, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

41. The article of claim 40, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture.

42. The article of claim 41, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture, wherein said metallization interconnect couples the transistors of the gate array architecture to form a flip-flop.

43. The article of claim 42, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture that connects the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

REMARKS

The above-referenced patent application is a continuation patent application of U.S. patent application serial no. 09/262,458, filed on March 4, 1999. In the aforementioned parent application, claims 27-43 have been allowed. Therefore, these claims are added to this continuation and cancelled in the parent to allow these claims to proceed to issuance without delay. Likewise, claims 1-26 in the above-referenced patent application are cancelled because these claims are being prosecuted in the parent application. No prosecution history estoppel results from any of these actions because it merely permits these claims to be prosecuted separately and, thereby, permits the allowed claims to issue. No claimed subject matter of any kind has been surrendered by these actions.

CONCLUSION

In view of the foregoing, it is respectfully asserted that the claims pending in this application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-0967. Consideration of this patent application and early allowance of these claims is respectfully requested.

Respectfully submitted,

Howard A. Skaist

Dated:

7/14/01

Howard A. Skaist
Senior Intellectual Property Attorney
Reg. No. 36,008

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

MARKED VERSION TO SHOW CHANGES

IN THE SPEC:

Insert the following paragraph at page 2, line 4:

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IN THE CLAIMS:

Cancel claims 1-26.

Please enter the following new claims:

27. An integrated circuit comprising: a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least one forming both N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P- type transistors;

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30. The integrated circuit of claim 27, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

31. The integrated circuit of claim 30, and further comprising an interconnect overlying said gate array architecture;

the interconnect being adapted to connect the transistors of the gate array architecture to form a flip-flop.

32. The integrated circuit of claim 31, wherein the interconnect is further adapted to connect the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

33. The integrated circuit of claim 32, wherein said gate array architecture is repeated in said integrated circuit.

34. The integrated circuit of claim 32, wherein said integrated circuit is incorporated in a communications device.

35. The integrated circuit of claim 32, wherein said integrated circuit is attached to a motherboard.

36. The integrated circuit of claim 35, wherein said integrated circuit is incorporated in a personal computer.

37. The integrated circuit of claim 36, wherein said personal computer comprises one of a laptop and a desktop computer.

38. An article comprising: a storage medium, said storage medium having instructions stored thereon, said instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least forming both N-type and P-type transistors;

wherein the transistors are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors;

the relatively-sized P-type diffusion regions being substantially adjacent;

successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions; and

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39. The article of claim 38, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

40. The article of claim 39, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

41. The article of claim 40, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture.

42. The article of claim 41, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture, wherein said metallization interconnect couples the transistors of the gate array architecture to form a flip-flop.

43. The article of claim 42, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture that connects the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.